

# LAYOUT GUIDE FOR DEMONSTRATION CIRCUIT 1682A

12-PORT PSE DAUGHTER CARD WITH DIGITAL ISOLATION

LTC4270/LTC4271

## DESCRIPTION

The LTC4270 and LTC4271 chipset, 12-port PSE, is a simplified solution as compared to the traditional quad PSEs. The LTC4270/LTC4271 solution reduces BOM cost and board space. To achieve this at the board level, parts placement and routing is critical. This layout guide highlights specific areas on a board layout requiring special attention and is best viewed in color print. Following these guidelines ensures optimal current reading accuracy, IEEE compliance, system robustness, and thermal dissipation. The DC1682A is used as an example LTC4270/LTC4271 layout and should be followed closely. Figures 1-6 provide reference for the DC1682A board layers.

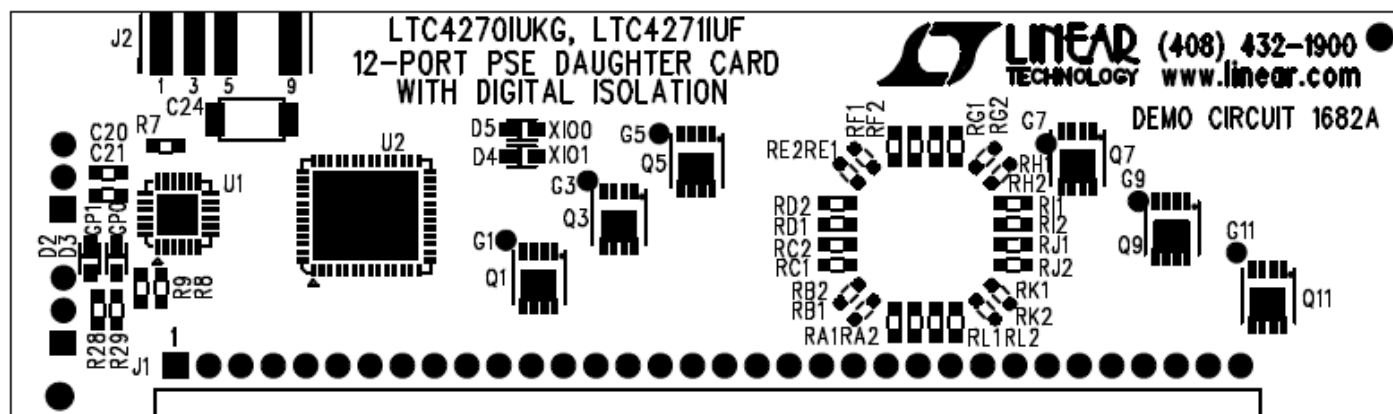


Figure 1. DC1682A Top Silkscreen and Components Placement

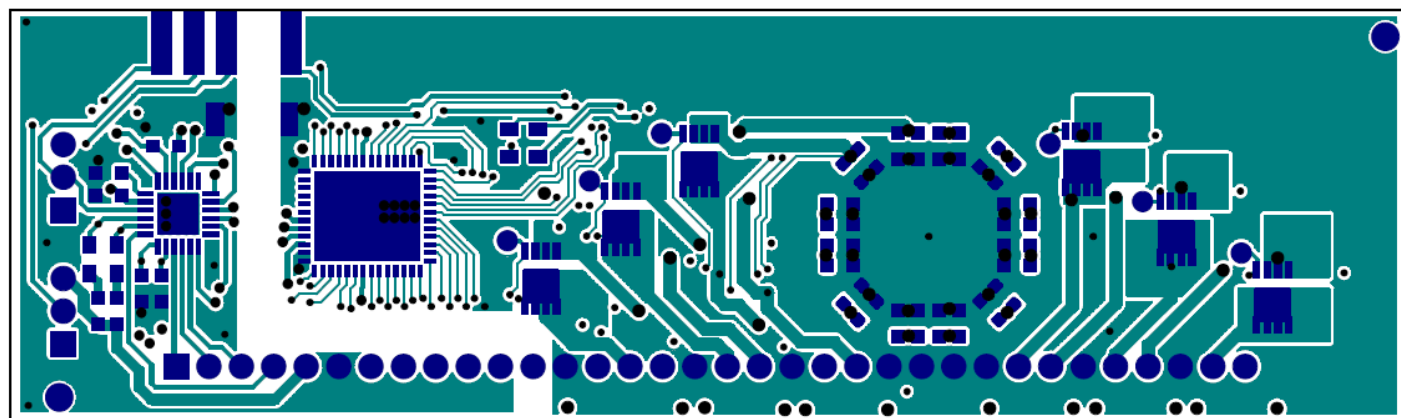


Figure 2. DC1682A Top Layer Routing

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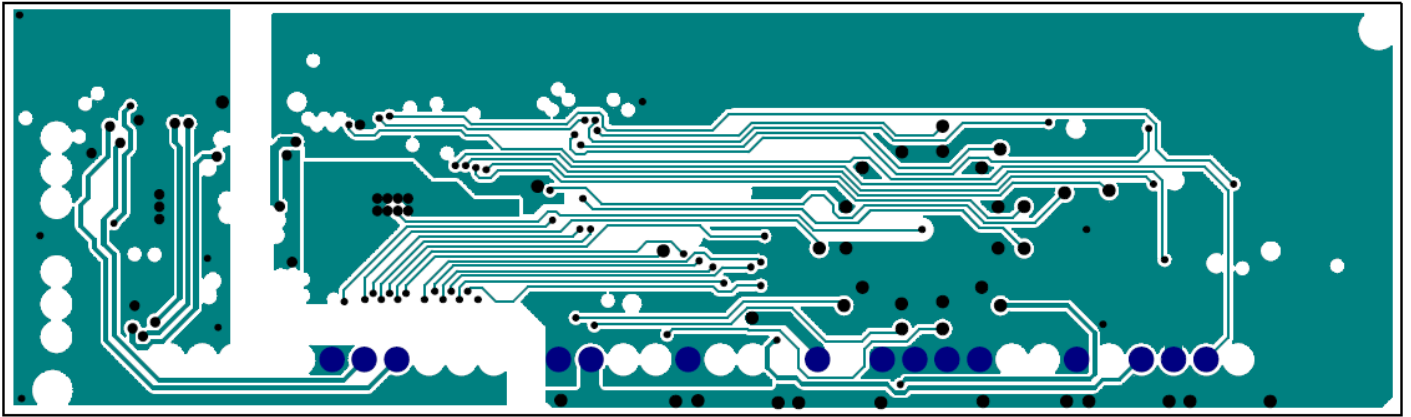


Figure 3. DC1682A Inner Layer 2 Routing

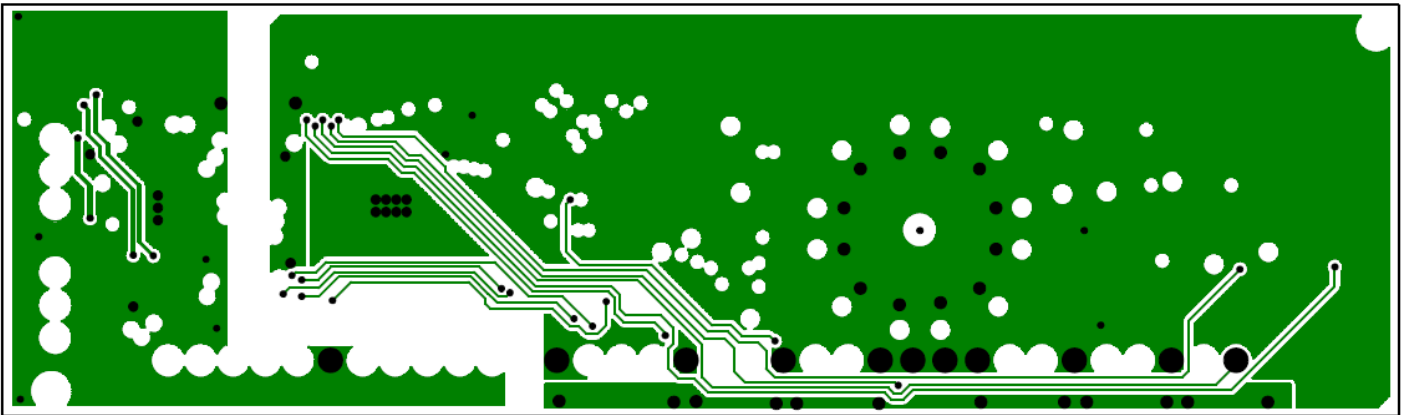


Figure 4. DC1682A Inner Layer 3 Routing

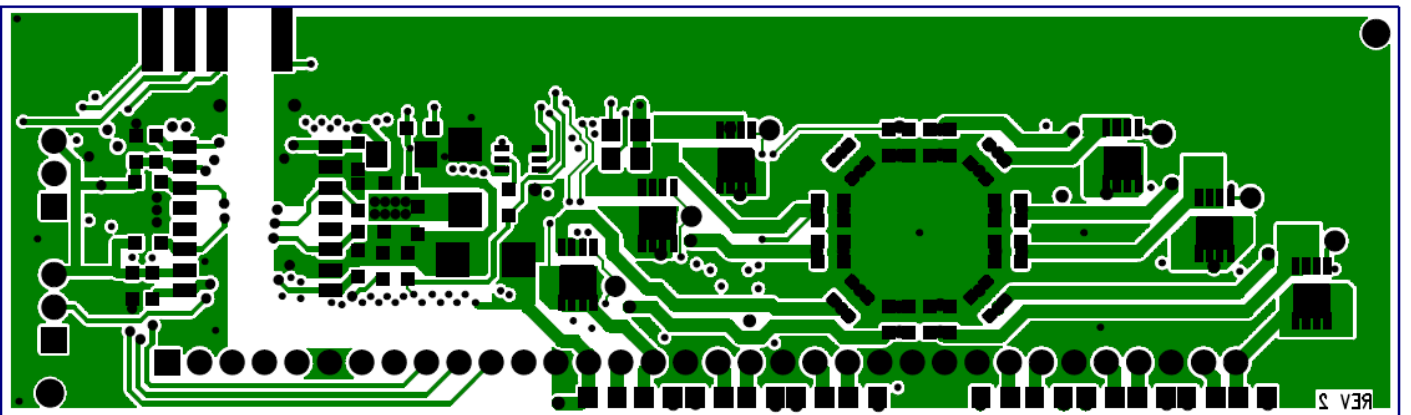


Figure 5. DC1682A Bottom Layer Routing



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## 12-PORT PSE DAUGHTER CARD WITH DIGITAL ISOLATION

### SENSE RESISTOR NETWORK CENTROID

Each port uses  $4 \times 1.00\Omega$  (referred here as resistor quad), 1%, sense resistors to provide the  $0.25\Omega$  sense resistance. The individual sense resistor package size is selected according to its power rating and the maximum DC current passed through the resistor. Each sense resistor will have a quarter of the total port current pass through it. For example, at 1A port current, 0.25A passes through each  $1\Omega$  resistor, thus requiring a rating of at least 1/16W.

All sense resistor quads must group together and tie in at one common point for the VEE connection. The distance from each sense resistor quad to the center must be as equal as possible. A circular configuration is best to provide this, creating a centroid network (Figure 7). The center area of the resistor network is filled with VEE copper (Figure 8). Each sense resistor quad has a common via that goes to an internal VEE plane (Figure 9).

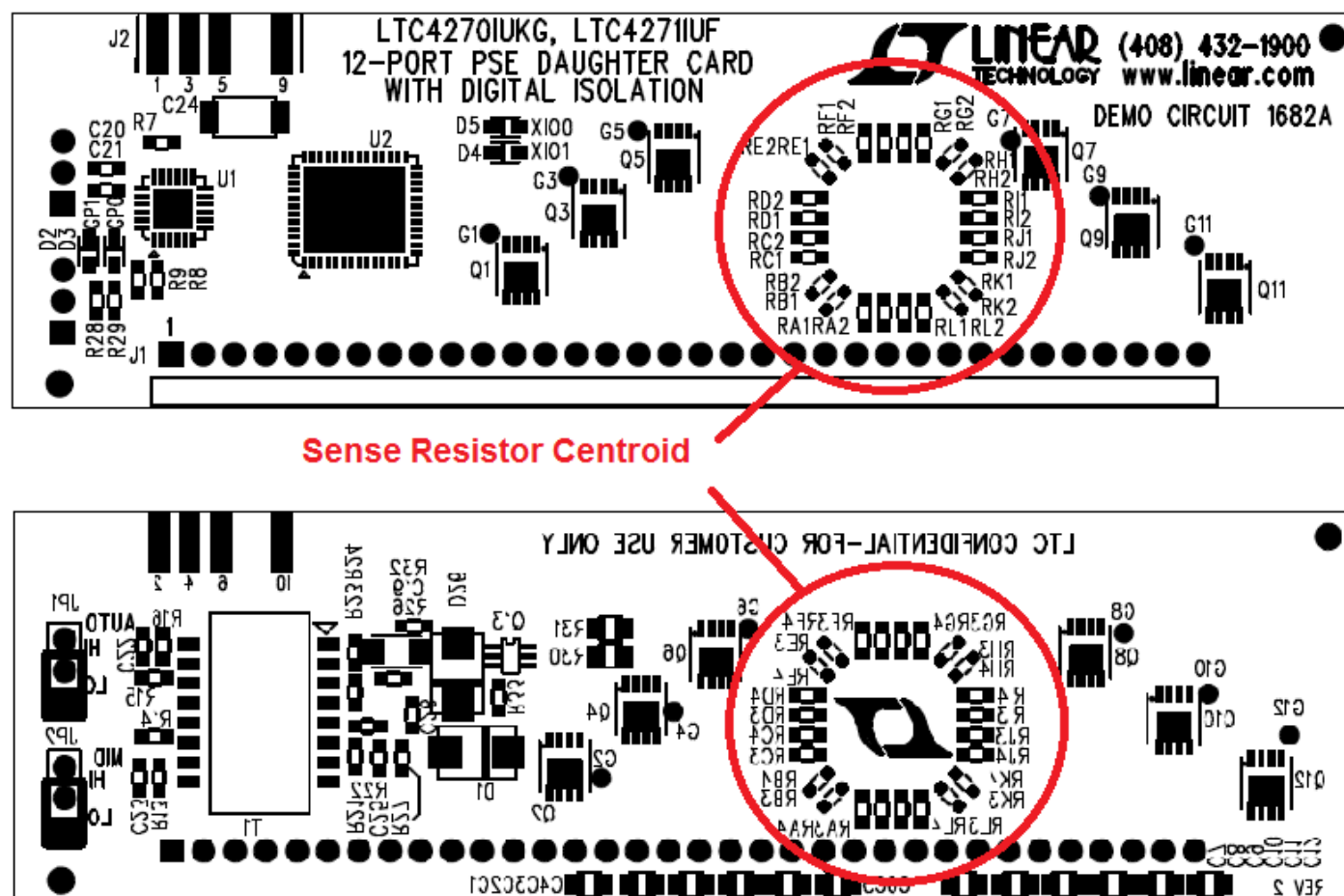
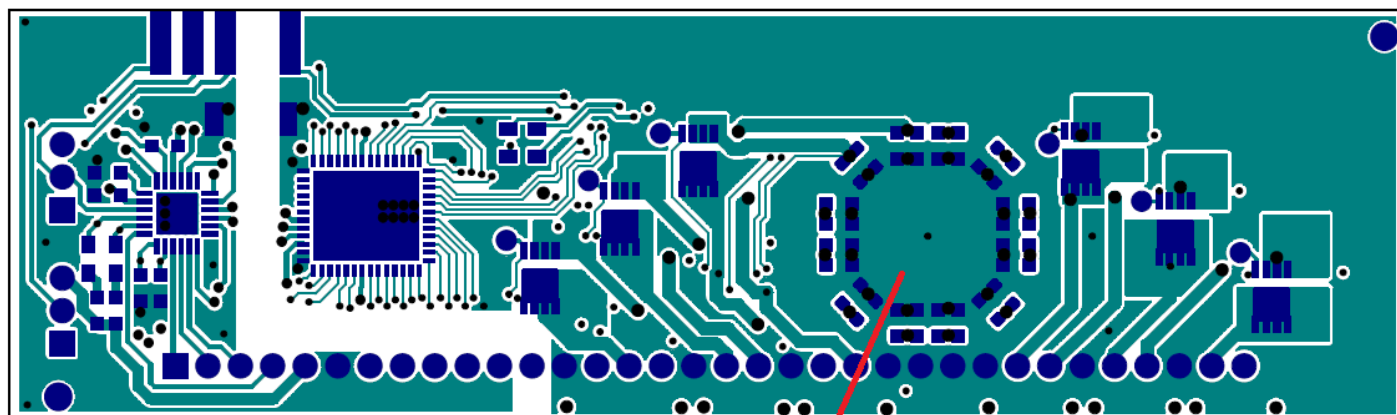


Figure 7. DC1682A Top and Bottom Silkscreen. The Sense Resistors are Grouped Together in a Centroid Configuration

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Sense Resistor Centroid Filled with VEE

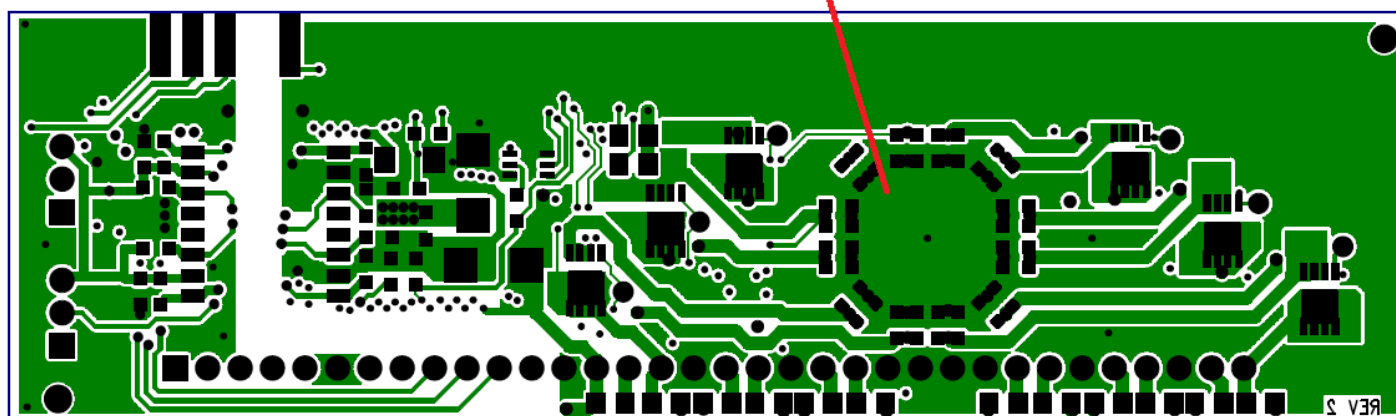


Figure 8. DC1682A Top and Bottom Layers. The Sense Resistors Centroid is Filled with VEE

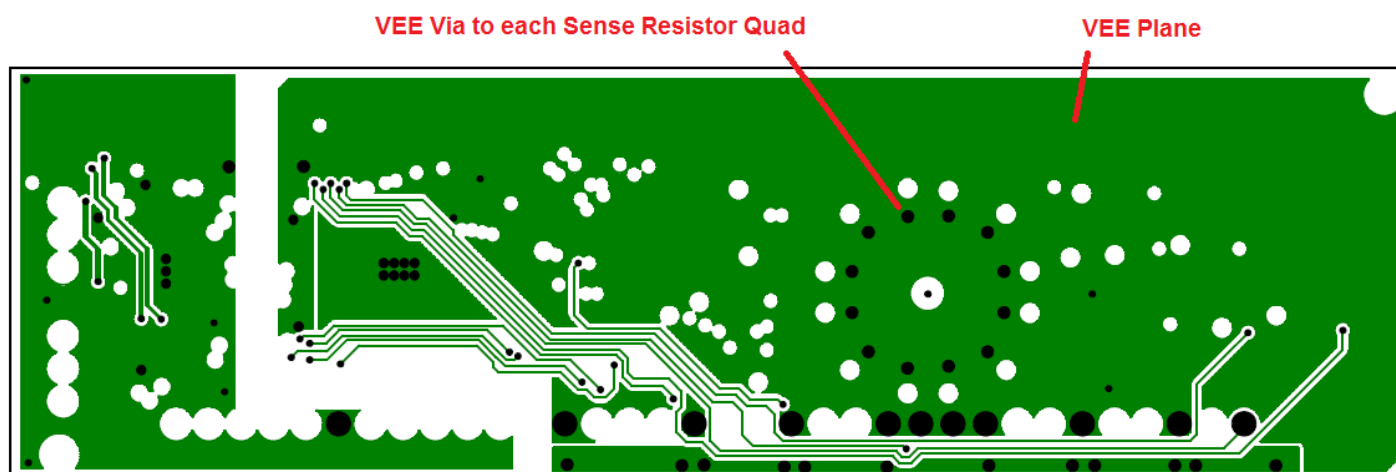


Figure 9. DC1682A Inner Layer 3. A Via to each Sense Resistor Quad Connects to the VEE Plane

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### VSSK AND SENSE PIN KELVIN SENSING

Each port has a SENSE pin at the LTC4270. An isolated Kelvin sense trace from the SENSE pin directly to the respective sense resistor quad is required (Figure 10). The power path trace between the MOSFET source and the sense resistor quad must be separate from the Kelvin sense trace.

VSSK is a Kelvin sense pin to VEE. This pin **MUST NOT** connect to a VEE plane. Instead, an isolated trace must go from the VSSK pin to the very center of the sense resistor centroid on the top and bottom layers (Figure 11 and Figure 12). This trace does not tie to the inner layer VEE plane (Figure 13).

Sense Trace goes from Sense Pin through Inner Layer Trace and Directly to the Sense Resistors

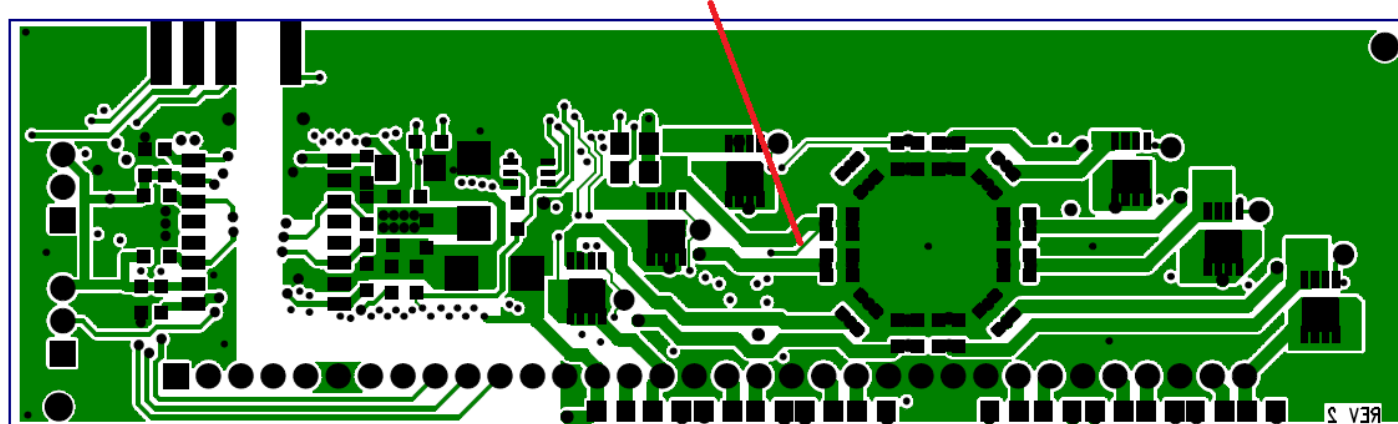


Figure 10. DC1682A Bottom Layer Routing. The Sense Trace Ties Directly from the Sense Pin to the Sense Resistor Quad

Via to VSSK Only Connects to Isolated Trace to Sense Resistor Centroid Center

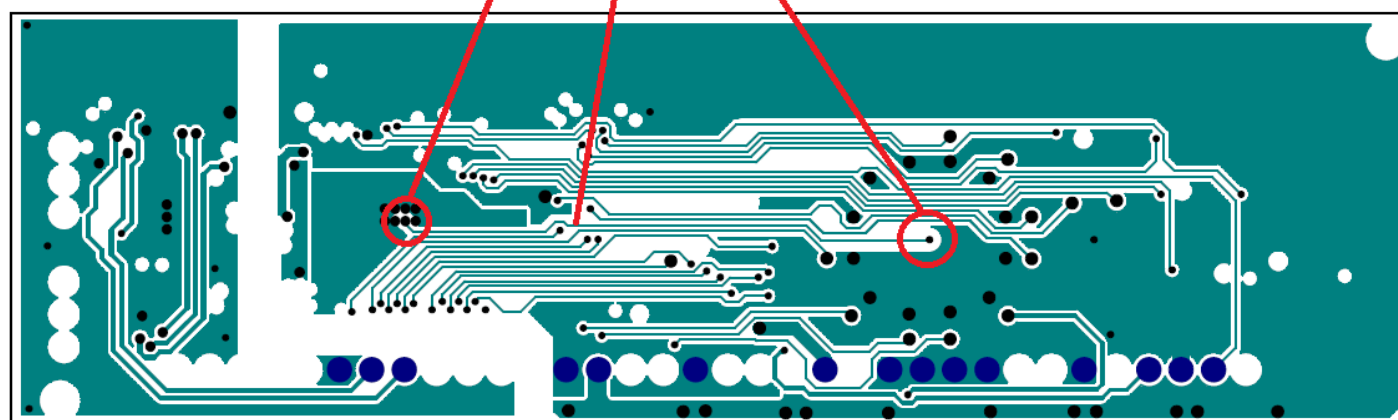


Figure 11. DC1682A Inner Layer 2. A Via to the VSSK Pin Connects an Isolated Trace to VEE at the Center of the Sense Resistor Centroid



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## 12-PORT PSE DAUGHTER CARD WITH DIGITAL ISOLATION

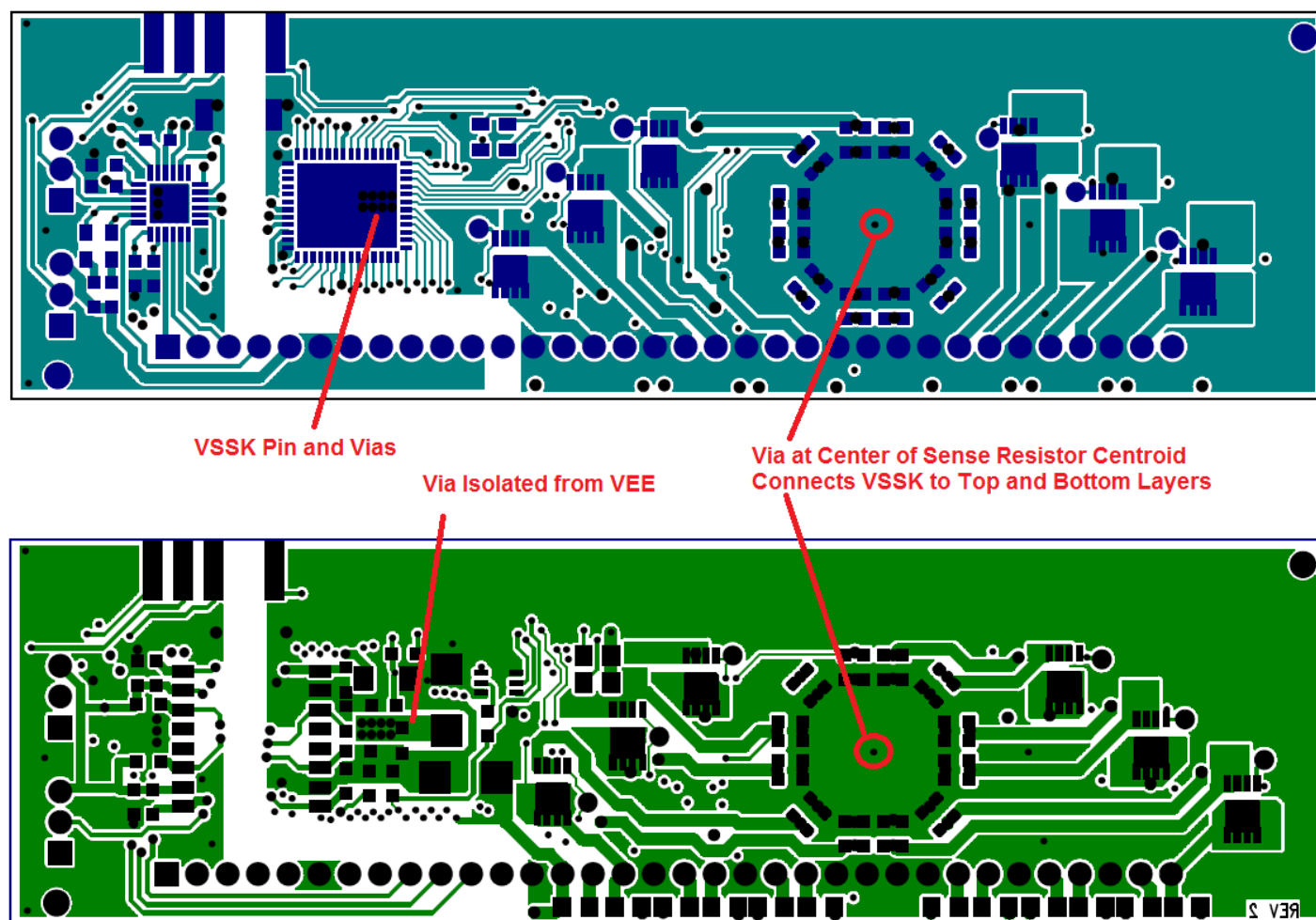


Figure 12. DC1682A Top and Bottom Layers. The Vias to the VSSK Pin Remain Isolated from VEE Copper Planes. The VSSK Trace to VEE Connects at the Center of the Sense Resistor Centroid on the Top and Bottom Layers

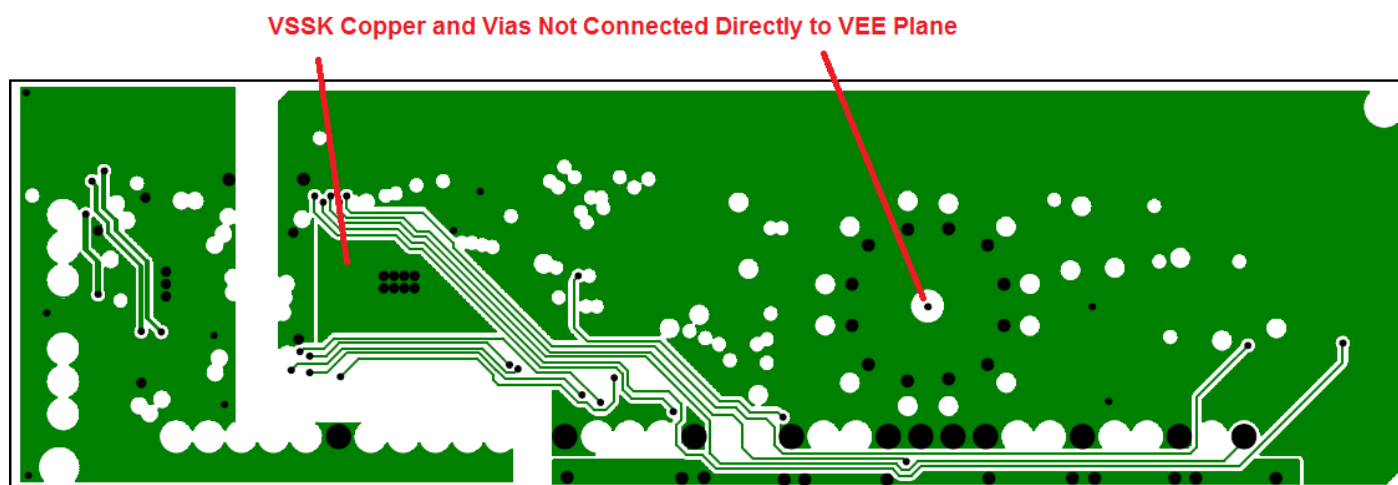


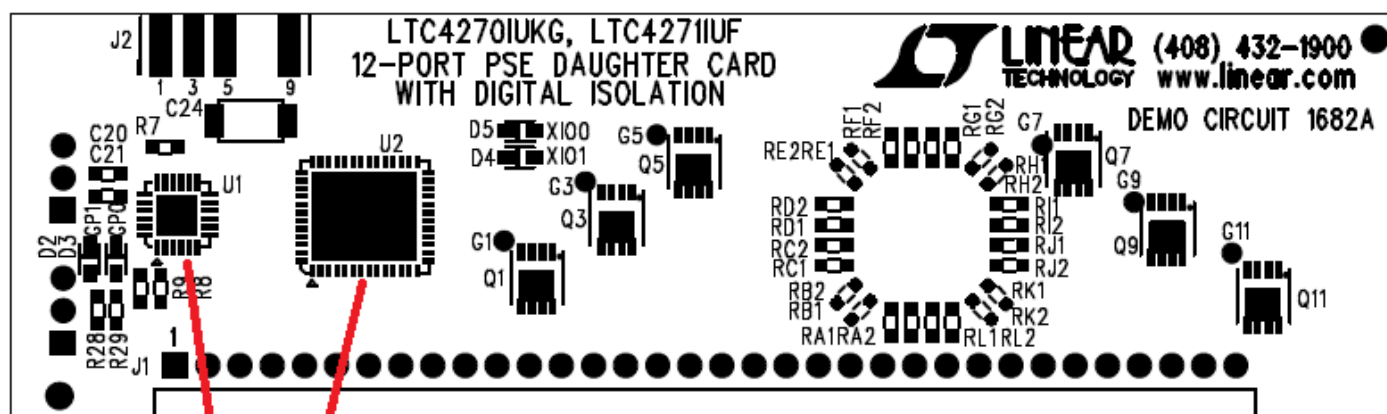
Figure 13. DC1682A Inner Layer 3. The Vias to the VSSK Pin do not Connect Directly to the VEE Plane. The Via at the Resistor Centroid is also Isolated from the VEE Plane

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## 12-PORT PSE DAUGHTER CARD WITH DIGITAL ISOLATION

### LTC4270/LTC4271 COMMUNICATIONS COMPONENTS LOCATION

The communications signals between the LTC4270 and the LTC4271 do not support long trace lengths. The LTC4270, the LTC4271, the transformer and the termination components must be next to each other with short trace length. The DC1682A places the LTC4270 and LTC4271 on the top side directly above the pins of the Ethernet transformer on the bottom side (Figure 14). The termination resistors and capacitors are placed next to the transformer pins.





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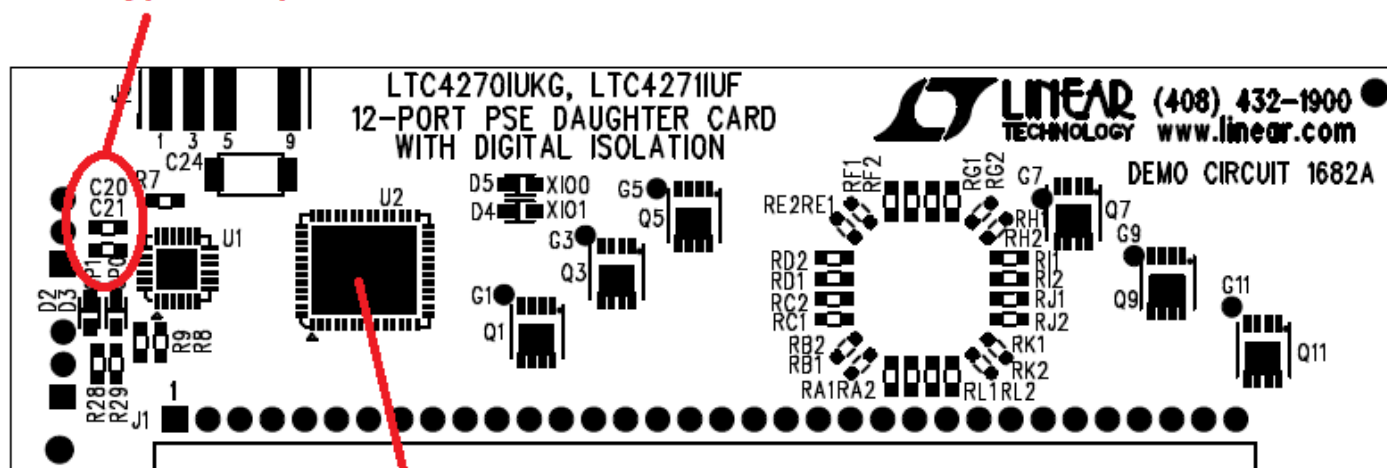
## 12-PORT PSE DAUGHTER CARD WITH DIGITAL ISOLATION

### PROTECTION DEVICES LOCATION

The TVS and bypass capacitors for VEE, CAP1, CAP2, and VDD33 must be close to the pins that they provide protection for (Figure 15).

The VSSK bypass capacitor and Schottky diode connect directly to the VSSK pin through a via and to a VEE plane. This capacitor and diode protect against any voltage offset between VEE and the VSSK Kelvin sense. Ensure VSSK remains isolated from any VEE plane and only connects to the sense resistor centroid.

#### Bypass Capacitors Close to the LTC4271



#### Protection Components (TVS and Bypass Capacitors) Directly Below the LTC4270

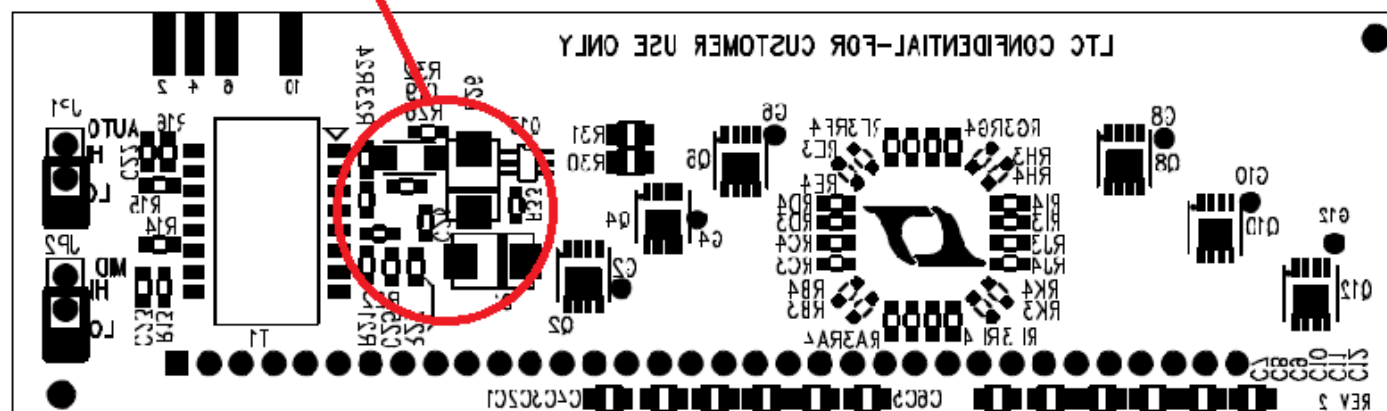


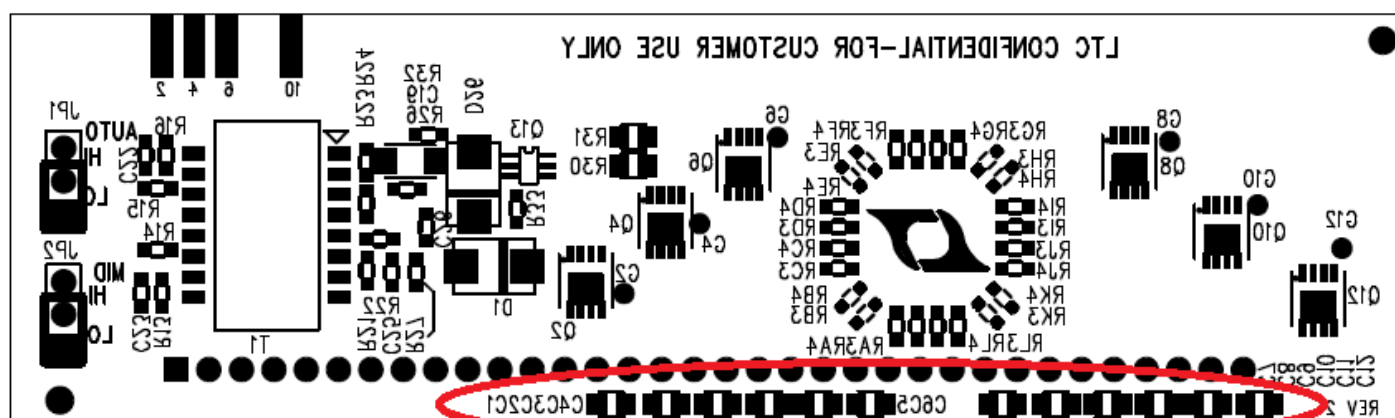
Figure 15. DC1682A Top and Bottom Silkscreen. The Protection Components (TVS and Bypass Capacitors) are Placed Close to the LTC4270 and LTC4271

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## 12-PORT PSE DAUGHTER CARD WITH DIGITAL ISOLATION

### OUT CAPACITORS

OUT capacitors are bypass capacitors for each OUT pin and must be close to the LTC4270 (Figure 16). These are NOT port capacitors and cannot be placed far from the LTC4270. Figure 17 shows a custom layout with a more ideal placement for OUT1 through OUT12 capacitors surrounding the LTC4270.



**Port OUT Capacitors as Close to the LTC4270 as Possible**

Figure 16. DC1682A Bottom Silkscreen. The OUT Capacitors are near the LTC4270

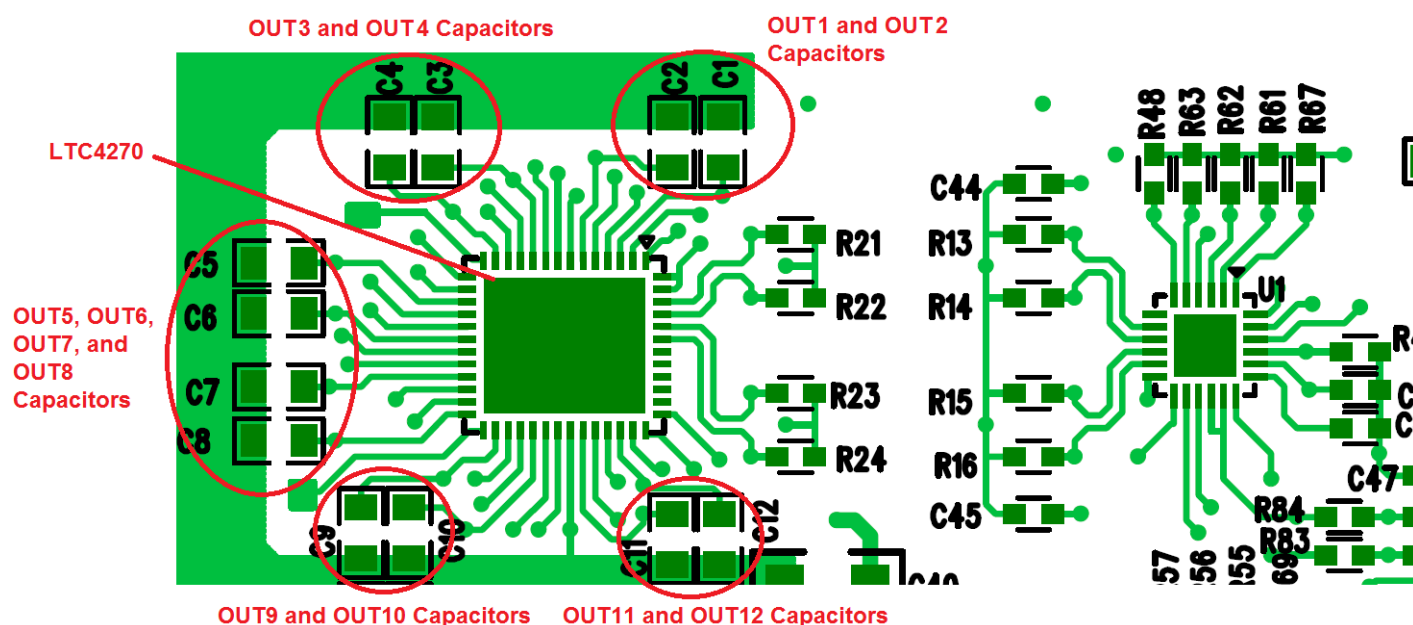


Figure 17. Custom Layout with Port OUT Capacitors Ideal Placement

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### ISOLATION REQUIREMENTS

Isolation between the LTC4270 and LTC4271 is maintained on all layers (Figure 18). A high voltage ground bypass capacitor is placed across the two grounds and next to the Ethernet transformer.

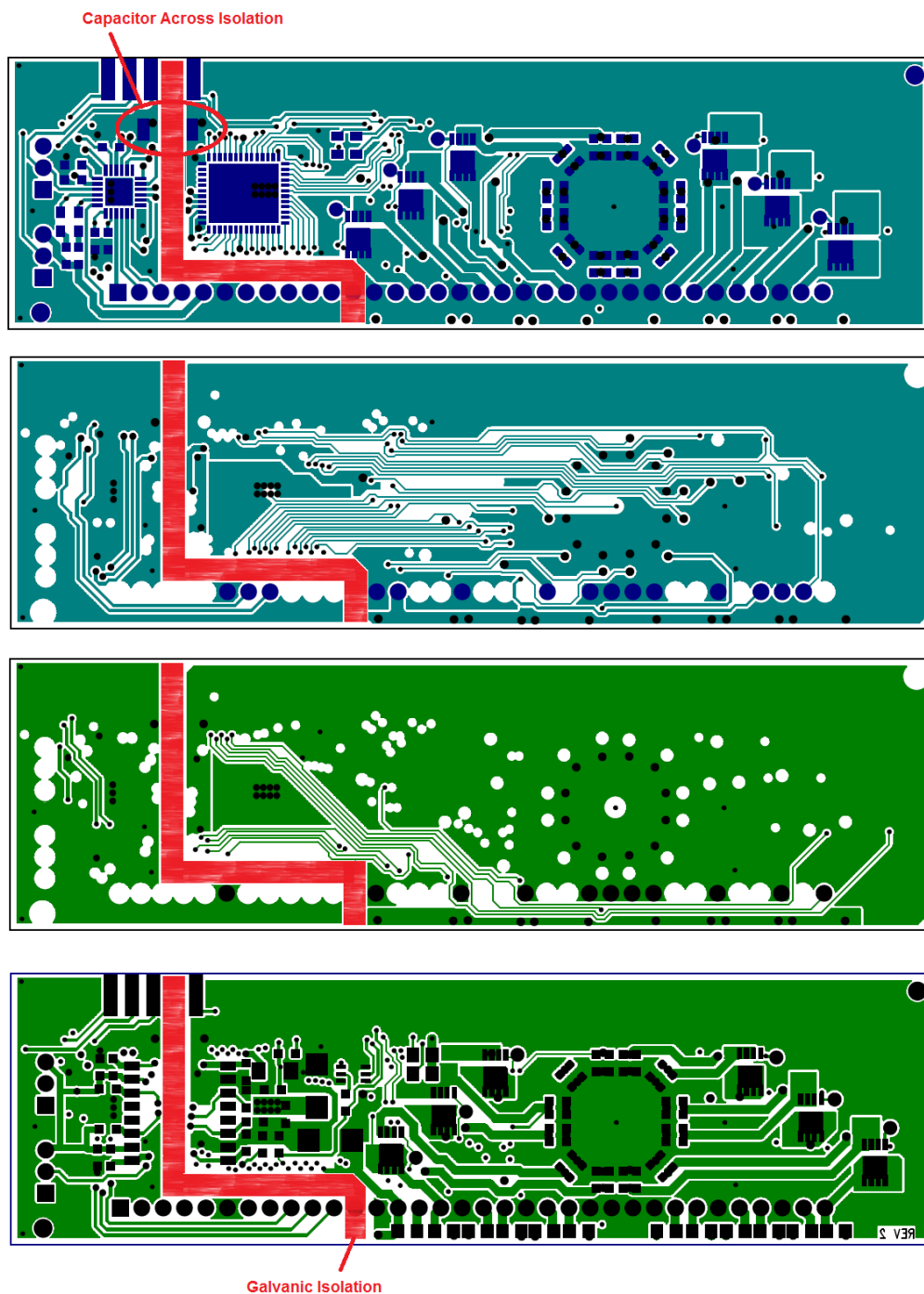


Figure 18. DC1682A Top, Layer 2, layer 3, and Bottom Layers. Galvanic Isolation is Maintained on Each Layer

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### POWER PATHS

High current paths are between the port output, the port MOSFET, the sense resistor quad, and VEE. Select a trace width and via size appropriate for the copper thickness that is capable of the maximum port DC current (Figure 19).

Provide sufficient copper from VEE supply to the sense resistor quads (Figure 20). If coming in from a mother board, similar to the DC1682A, reserve enough pins for VEE for to handle the total maximum current.

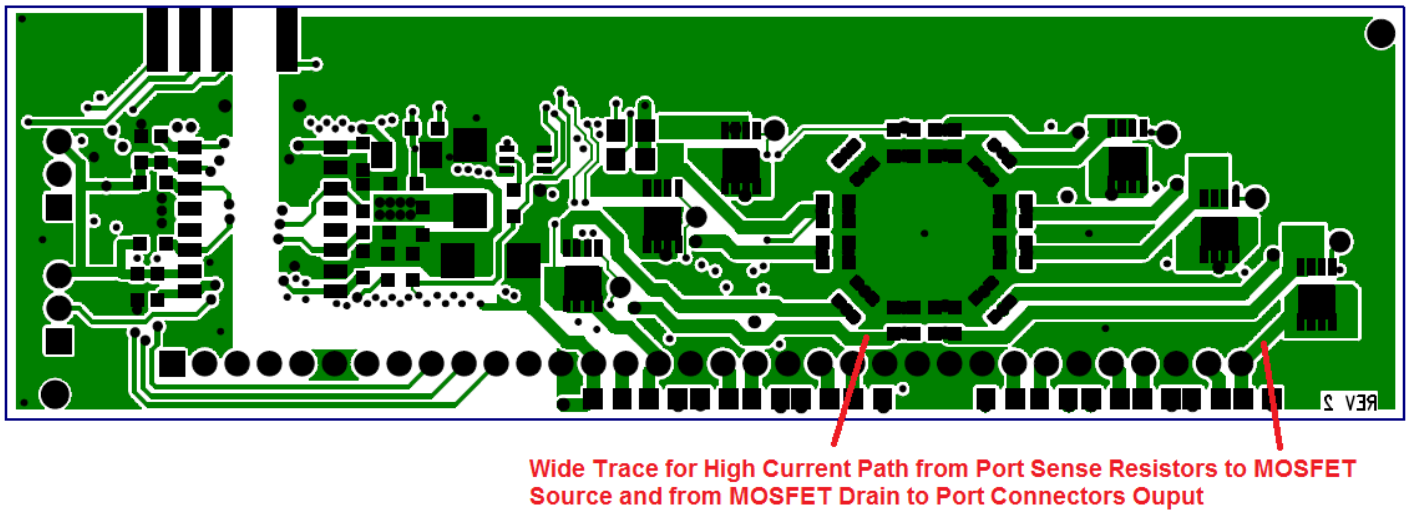


Figure 19. DC1682A Bottom Layer. Wide Traces are used for High Current Paths

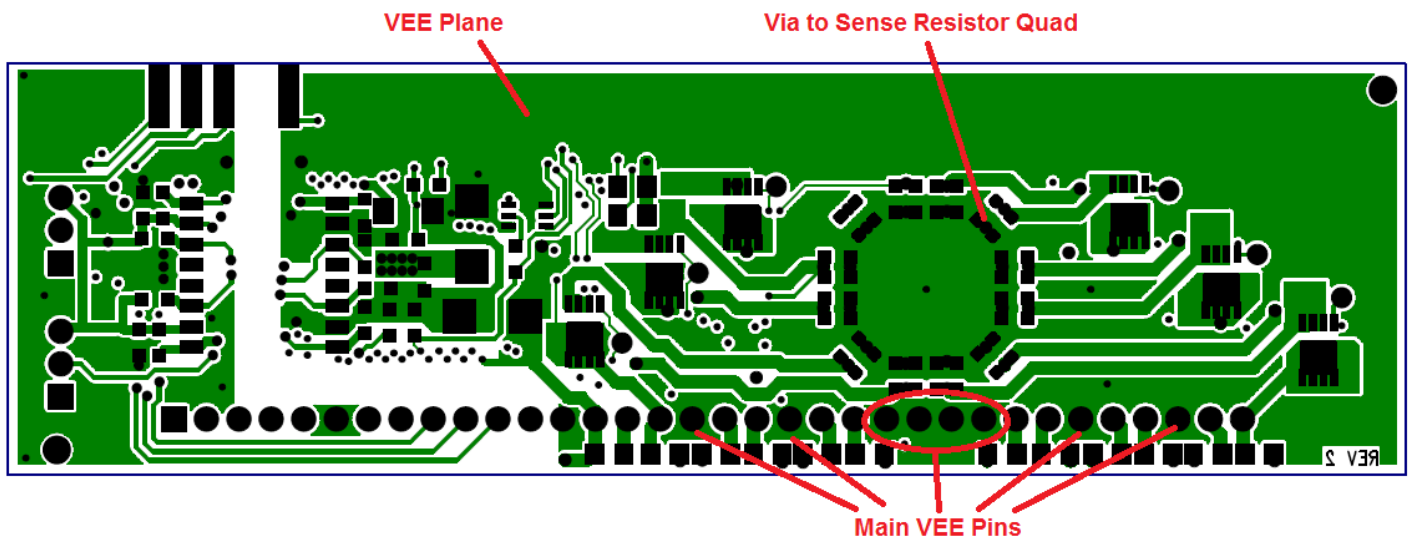


Figure 20. DC1682A Bottom Layer. The 34-Pin Connector has Enough Pins Reserved for VEE to Handle the VEE Current

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### 2 OUNCE COPPER ALL LAYER

All layers (top, bottom, and inner layers) must have 2oz copper thickness or more.

### THERMAL CONSIDERATIONS

There are three main heat sources on the 12-port daughter card: the MOSFETs, the sense resistor quads, and the LTC4270. Thermal relief and spreading should be considered. Use techniques such as large copper areas under the solder pads, alternating and spreading out the MOSFET locations. Fill areas with copper for VEE. Dissipate the heat under the LTC4270 VSSK solder paddle to other layers. Figure 21 shows the board layers for the DC1682A as an example of good copper fill. On this board, any open area is filled with copper to help spread heat throughout the board. Multiple vias under the VSSK paddle connect to isolated copper on the inner layer and bottom layer for heat sinking.

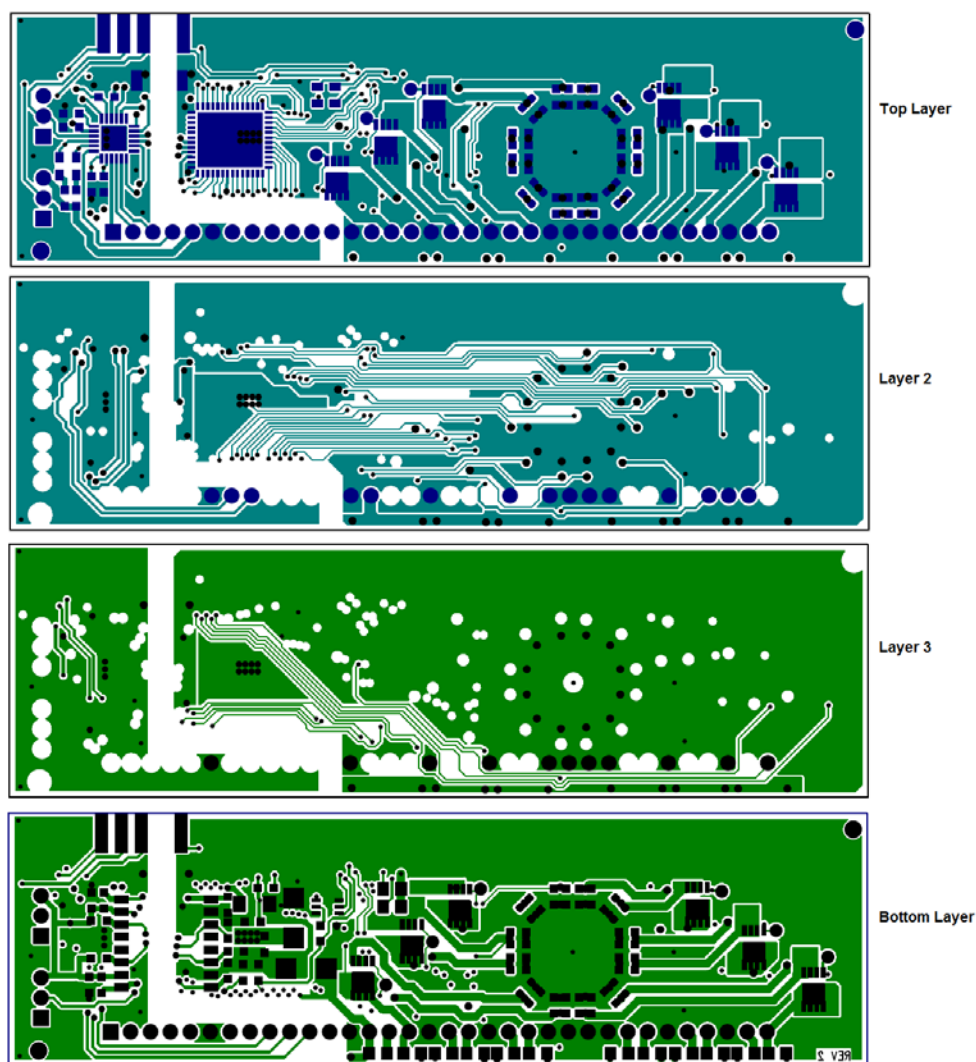


Figure 21. DC1682A Layers 1 through 4 with Copper Fill and VSSK Heat Sink

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### LTC4270/LTC4271 Layout Checklist:

- Sense resistors are placed equal distance from a common VEE point
- Center of sense resistor centroid is filled with VEE copper
- Via at the VEE side of each sense resistor quad going to a VEE plane
- An isolated VSSK trace from the VSSK pin ties directly to center of sense resistor centroid and not connected to a VEE plane
- SENSE pins go directly to the respective sense resistor quad
- LTC4270, LTC4271, Ethernet transformer and termination components are next to each other
- Protection components are close to the LTC4270 and LTC4271
- OUT capacitors are near the LTC4270
- Power paths have wide traces
- VEE has sufficient copper
- At least 2oz copper on all layers
- Areas filled with copper to spread heat out and VSSK has isolated vias going to isolated copper